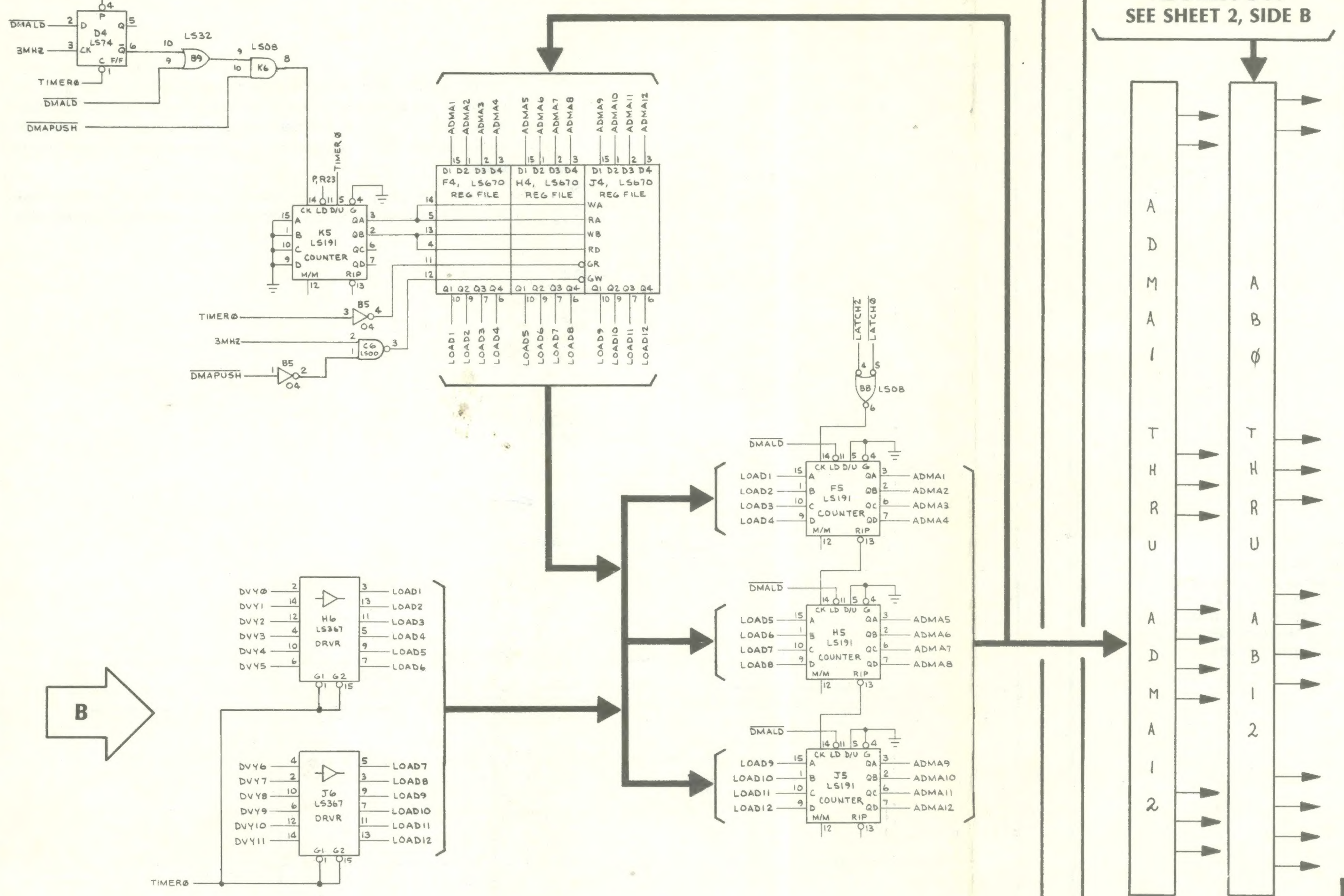
DISPLAY CONTROLLER

FROM MICROCOMPUTER ADDRESS BUS SEE SHEET 2, SIDE B

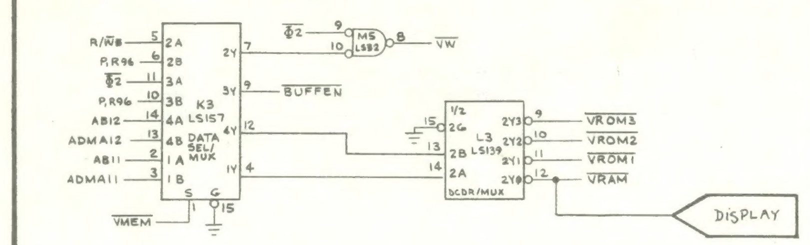


Counters F5, H5, and J5 contain the address of the next instruction to be fetched from memory. They are incremented one count each time information is loaded into data latch 0 or latch 2.

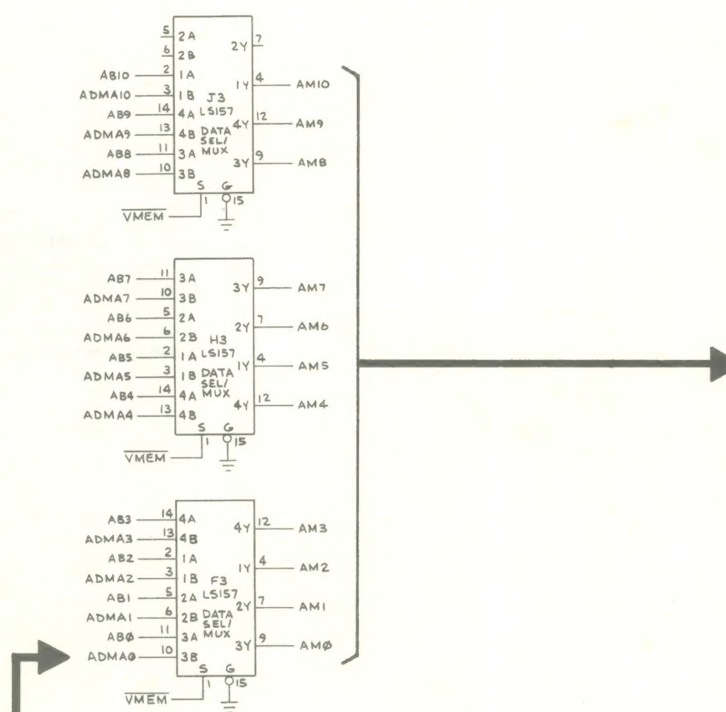
New locations may be loaded into the program counter when DMALD goes low. The information may be loaded either from the data latches through buffers H6 and J6 when TIMER0 is low. When TIMER0 is high, the program counter is loaded from the stack (F4, H4, and J4).

The stack is a 4-word, 12-bit memory, used to save the contents of the program counter for future reference. It is loaded when DMAPUSH is low. Immediately after information is written into the stack, counter K5 increments one count. Immediately before loading the program counter from the stack, counter K5 decrements one count.

ADDRESS DECODER



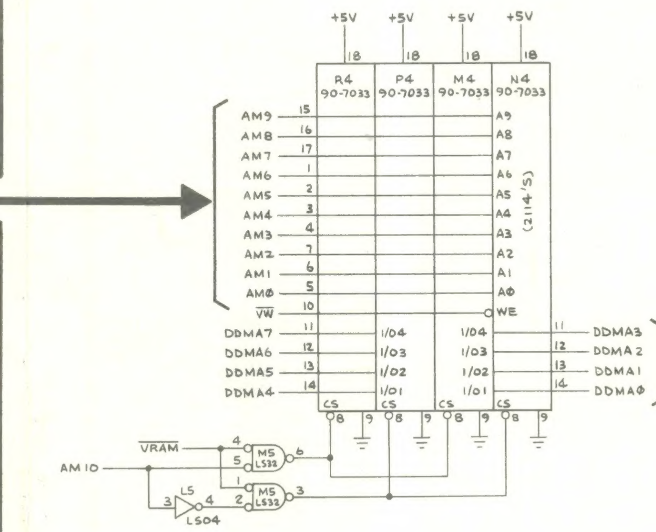
ADDRESS SELECTOR



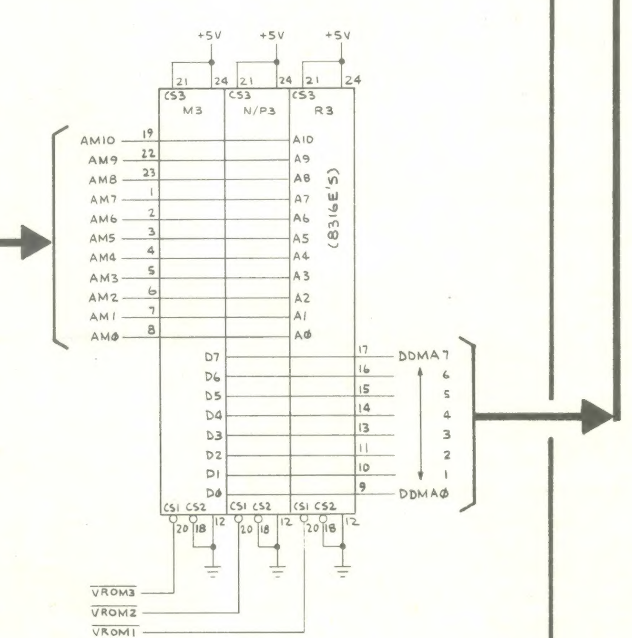
The address selector consists of multiplexers F3, H3, J3 and K3. When VMEM is low, the MPU of the microcomputer gains access to the address inputs of the vector generator memory. In this state, BUFFEN is from Φ2 and VW (vector generator write) is low when Φ2 and R/WB are both low. When VMEM is high, the address input to the vector generator memory is from the vector generator program counter and state machine. In this state, BUFFEN and VW are both held high by the pullup resistors connected to the 2B and 3B inputs of multiplexer K3.

Address decoder L3 decodes address bits A11 and A12, and selects the RAM or one of three ROMs of the program memory.

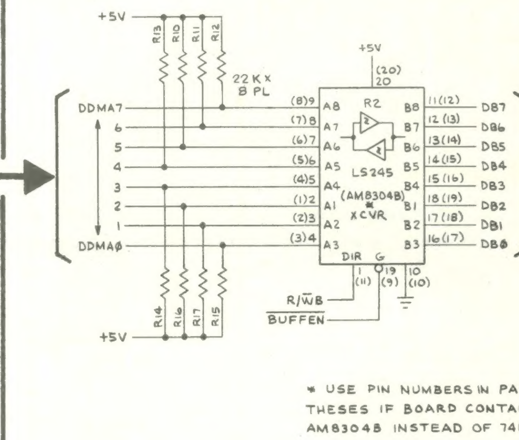
VECTOR GENERATOR RAM



VECTOR GENERATOR PROGRAM MEMORY



VECTOR GENERATOR DATA BUFFER



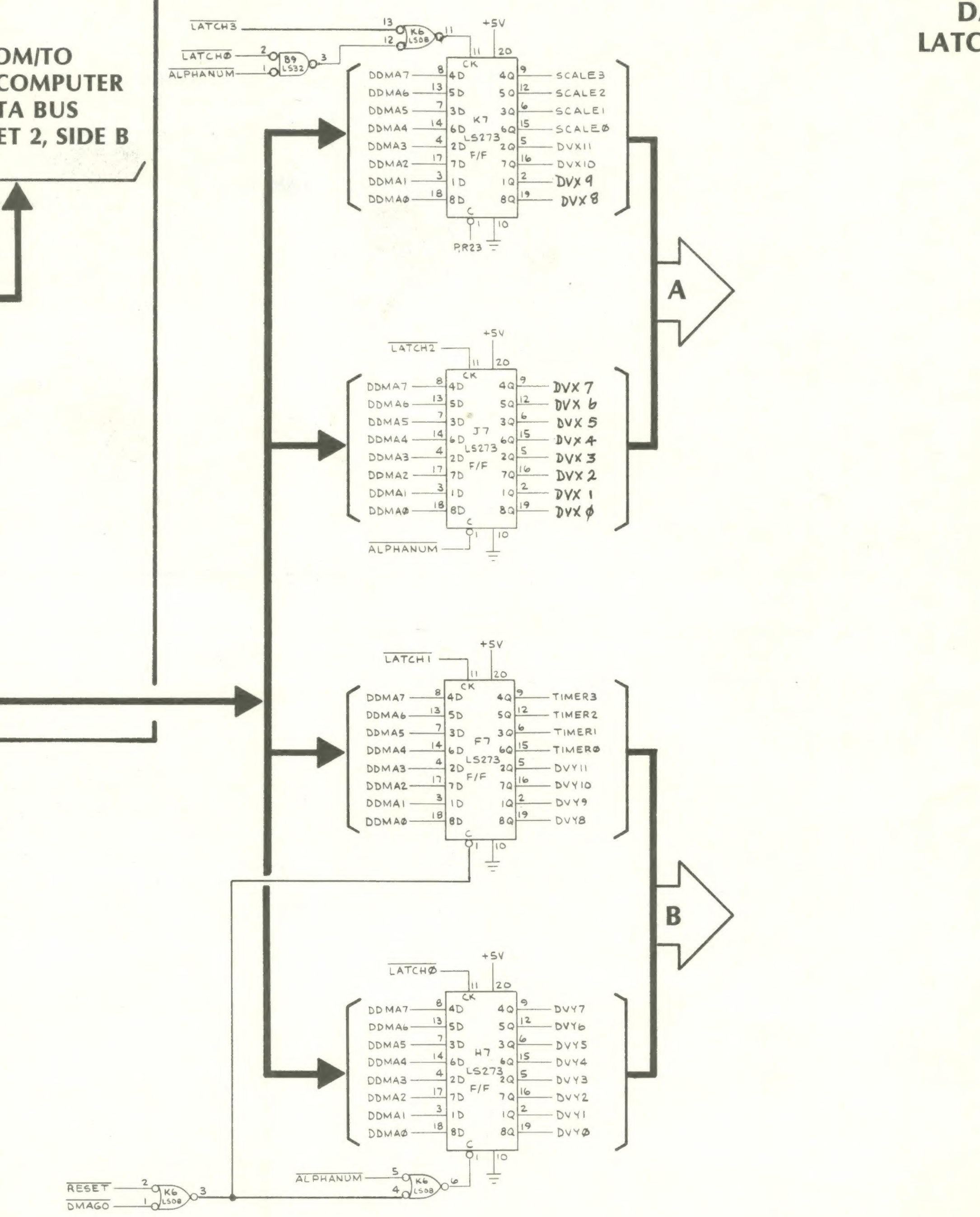
* USE PIN NUMBERS IN PARENTHESES IF BOARD CONTAINS AM8304B INSTEAD OF 74LS245

FROM/TO MICROCOMPUTER DATA BUS SEE SHEET 2, SIDE B

The vector generator memory consists of 2K of RAM and 6K of ROM. It may be directly accessed by the MPU of the microcomputer through the direct memory access process (DMA). Data is written in from the microcomputer thru data buffer R2 when BUFFEN and R/WB are low.

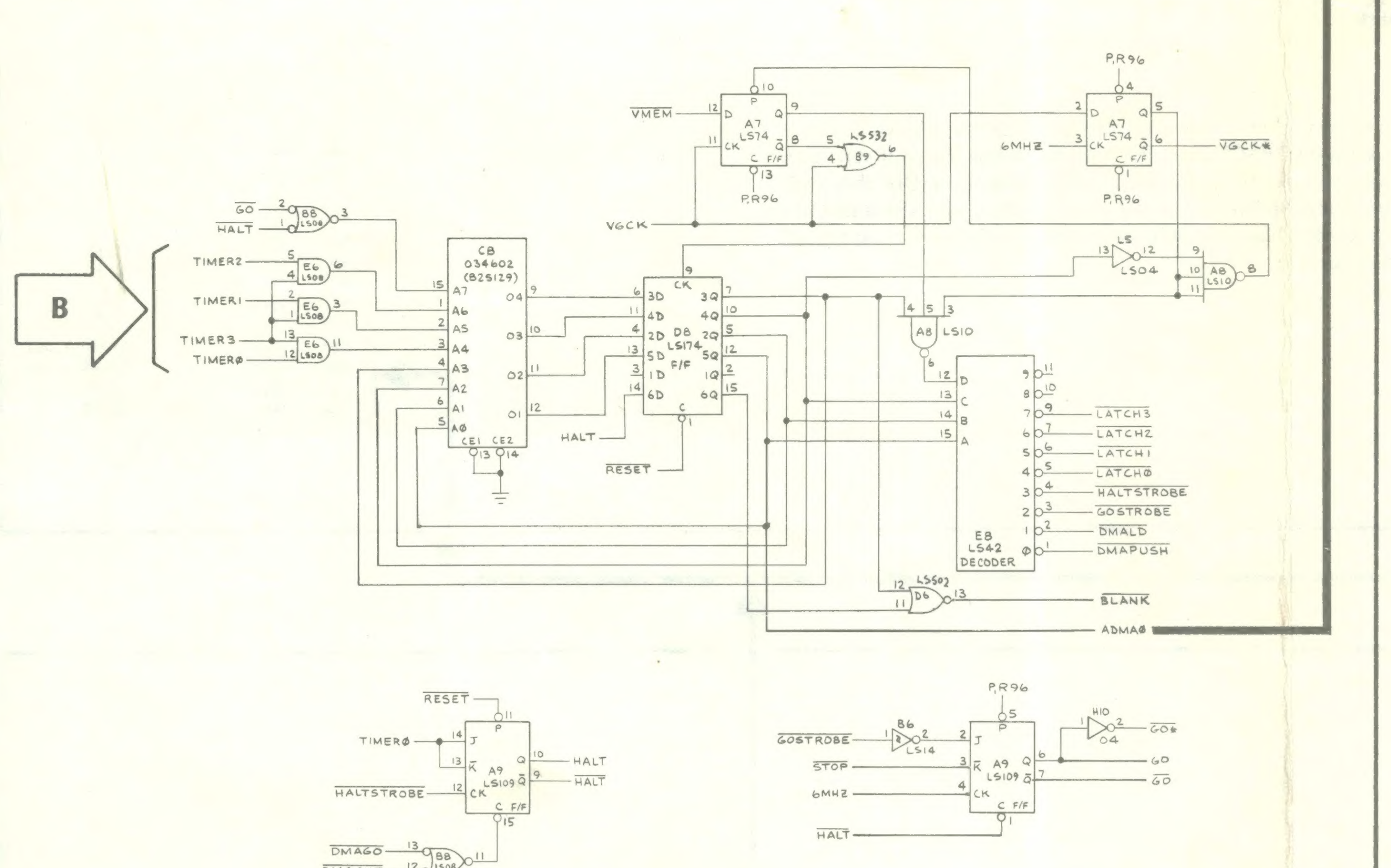
Any one of the three 2K×8 vector generator program memory chips M3, N/P3, or R3 may be substituted with two equivalent 1K×8 chips in locations K4 and L4. See the Illustrated Parts Catalog, Chapter 5, of the game manual for equivalent part numbers.

DATA LATCHES



The data latches consist of latch 0 (H7), latch 1 (F7), latch 2 (J7), and latch 3 (K7). Inputs DDMA0 thru DDMA7 are the data outputs from the vector generator memory.

Latches 0 thru 2 are directly clocked by the rising edge of the LATCH0, LATCH1, and LATCH2 outputs from the vector generator's state machine. Latch 3 is clocked by LATCH3 or by LATCH 0, if ALPHANUM is low. Latch 0 is cleared when RESET, DMAGO, or ALPHANUM goes low. Latch 1 is cleared if RESET or DMAGO is low. Latch 3 is cleared by ALPHANUM.



STATE MACHINE

The state machine consists of input gates B8 and E6, ROM C8, latch D8, clock circuitry A7, and decoder E8. Four bit input TIMER0 thru TIMER3 is the operation code input to the state machine. The A4 thru A6 address input to ROM C8 tells the ROM which instructions to perform. Address inputs A0 thru A3 from latch D8 tells the ROM which state was last performed. The address A7 input GO tells the ROM that the position counters are presently drawing a vector. The HALT input to A7 tells the ROM that the vector generator has completed its operations.

During initial power up of the game, the HALT signal is preset low. The microcomputer reads the high HALT signal through its switch input port (buffer M10) on data line DB0. This tells the microcomputer that the vector generator is halted and waiting for an instruction. To ensure that the beam is off when the state machine is halted, the high HALT, clocked through latch D8, results in a low BLANK to the Z axis output.

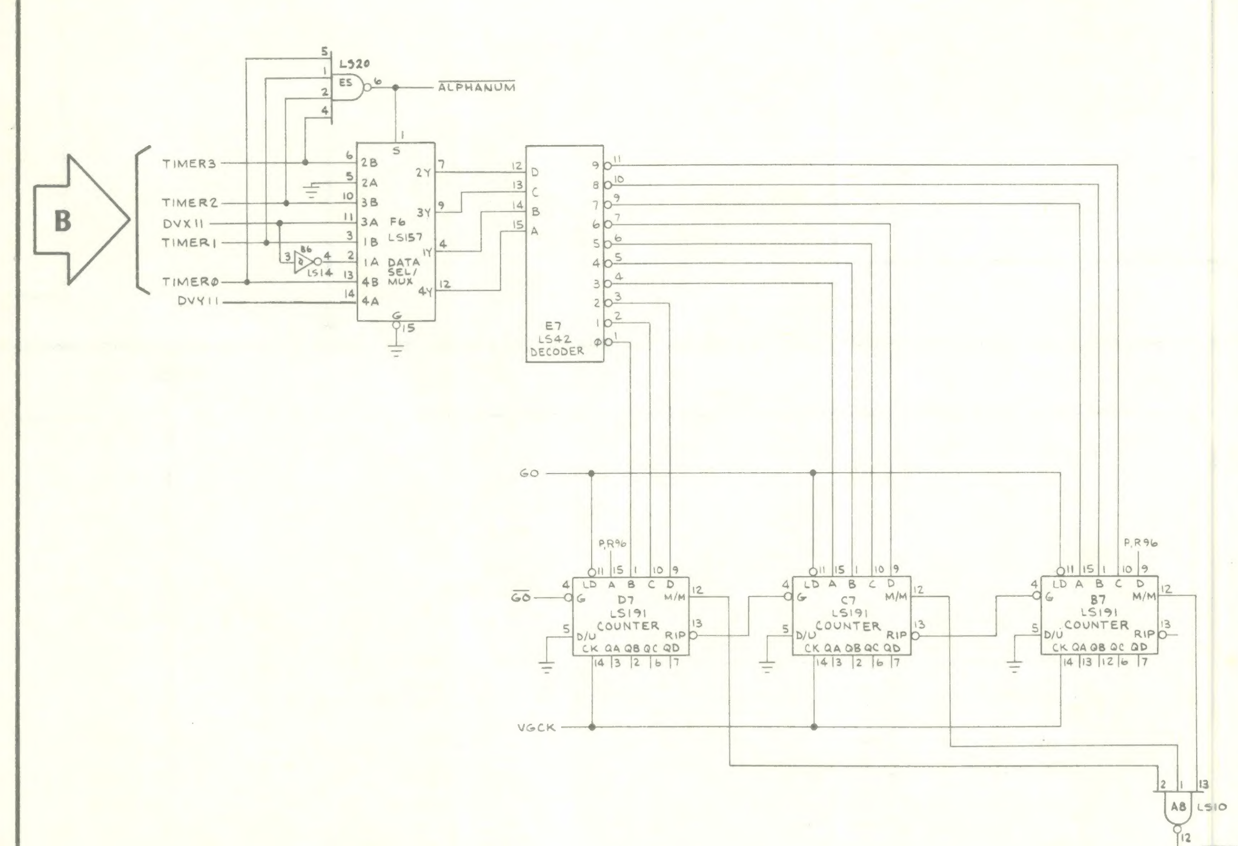
The microcomputer outputs an address that results in a DMAGO signal that causes HALT to go high, and clears the vector generator data latches. This makes TIMER0 thru TIMER3 signals all low.The state machine now begins executing instructions, starting at vector memory location 0.

When the state machine receives the operation code for a HALT instruction, it outputs a low HALTSTROBE, setting the HALT flip-flop A9, and suspending state machine operation.

The GO signals loads and enables the vector timer and the X and Y position counters and tells the ROM that the vector generator is now actively drawing a vector. The HALT input to GO flip-flop A9 sets the outputs to ensure that the vector timer and position counters are not active when the state machine is halted. When a low GOSTROBE is clocked through A7, the vector timer and X and Y position counters begin to operate from the GO, GO and GO* signals. When STOP is clocked through A7, the vector timer has reached its maximum count, and GO goes high. This means the vector has been drawn.

The VGCK input to the clock circuitry is a buffered 1.5 MHz clock signal from the microcomputer. This is the same frequency used to clock the MPU of the microcomputer. The signal clocks latch D8 unless the microcomputer is addressing the vector RAM or ROM memories, when VMEM goes low. Then the clock input to latch D8 goes high and stays high until VMEM goes high. However, if decoder E8 isn't outputting a latch strobe, the pin 10 preset input to A7 will maintain the clock input to latch D8.

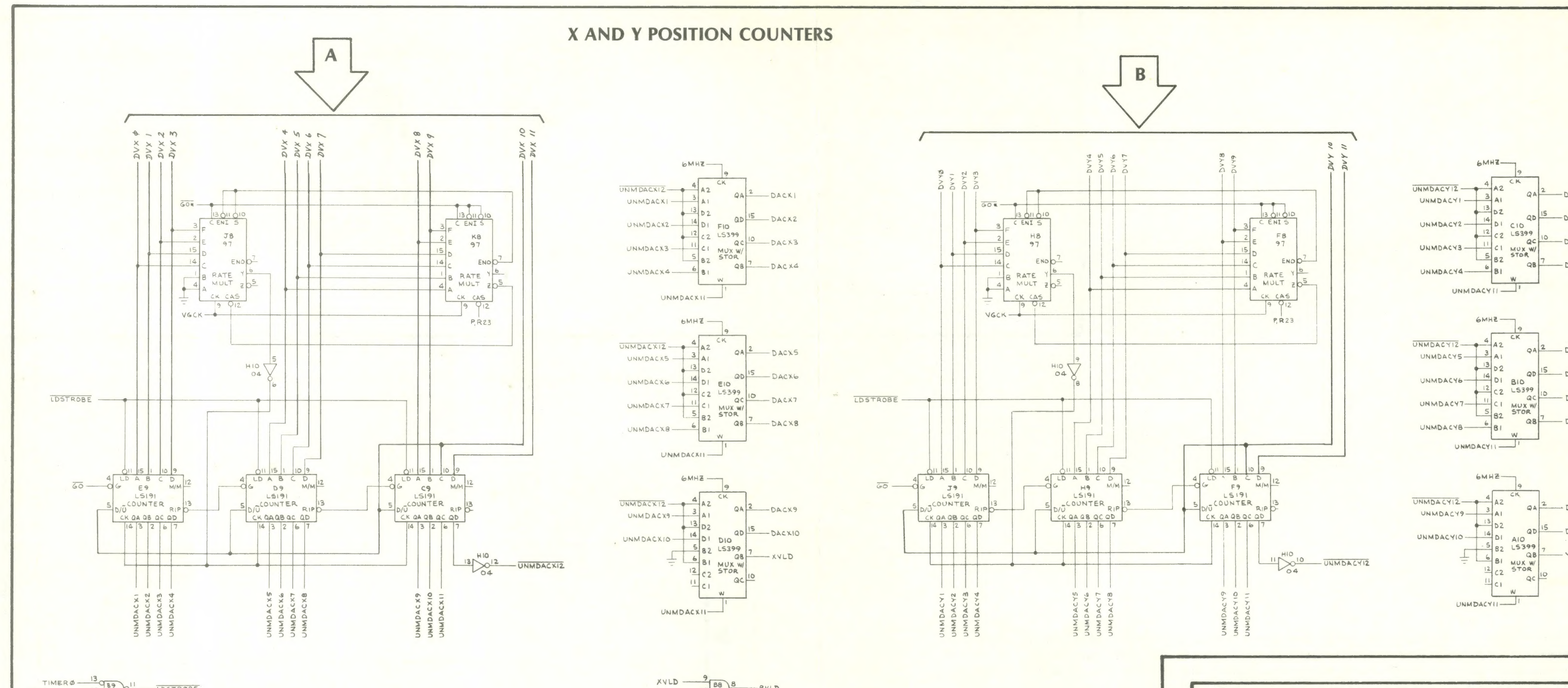
VECTOR TIMER



The vector timer consists of multiplexer F6, decoder E7, and counters B7, C7, and D7. If TIMER0 thru TIMER3 inputs are any state but all high, decoder E7 directly decodes the signals and loads the decoded low into one of the counters. When GO goes low, the counters count from the loaded count until the counters all reach their maximum count. This count is a maximum of 1024. At this time STOP goes low and clears the GO flip-flop of the state machine.

If the TIMER signals are all high, ALPHANUM goes low and data signals DVX11 and DVY11 are decoded by decoder E7. With this input the counter's maximum count is 64.

X AND Y POSITION COUNTERS



The X and Y position counters are two exactly identical circuits. Therefore, the following description only discusses the X position counters.

The X position counters contain rate multipliers (J8 and K8), down/up counters (C9, D9, and E9), multiplexers (D10, E10, and F10), and associated gates (B8 and H10). The rate multipliers divide the VGCK input by a factor equal to the DVX inputs to the rate multipliers. The resulting divided VGCK clocks the counters. The counters count for the amount of time as allowed by the vector timer through the GO flag of the state machine.

When TIMER0 and HALTSTROBE are both low, LDSTROBE goes low. This allows the DVX signals from the vector generator data latch to be loaded into the counters. When GO and GO* from the GO flag of the state machine go low, the rate multipliers begin to operate and the counters begin to count from the loaded number. If DVX10 is low, the counters count up. If high, the counters count down.

The UNMDACX1 thru UNMDACX10 (X axis unmultiplexed digital-to-analog converter signals) are transferred and stored at the output of the multiplexers on each rising edge of the 6 MHz clock (from the microcomputer clock circuitry). The DACX1 thru DACX10 signals are sent to the digital-to-analog converters (DACs) in the X video output.

The DACX1 and DACX10 outputs represent the physical placement of the beam on the monitor. The far left of the monitor screen is 0, the center is 512, and the far right is 1,023. Therefore, if the DACX1 thru DACX10 signal was greater than 1,023, the monitor beam would go off the right side of the screen and start again on the left side of the screen, a "wrap around" condition. To prevent a wrap around, the multiplexers' select input from UNMDACX11 goes high when the count is greater than 1023 or less than 0. This selects UNMDACX12 to be output from the multiplexers to the DACs, forcing all zeroes or all ones.

The XLD and YLD (X and Y valid) outputs from the X and Y position counter multiplexers are gated together to enable the Z axis output.

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